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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,764	08/02/2004	Hong-Gee Fang	11425-US-PA	4763

31561 7590 11/16/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
GOODLEY, JAMES E	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,764	FANG ET AL.	
	Examiner	Art Unit	
	James E. Goodley	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/2/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 and 4-26 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Nakajima et al (US 6,114,917)***.

Regarding **claims 1, 2 and 20**, lines 17-41 of column 5 and Fig. 2 of Nakajima shows:

a low power consumption oscillation circuit [5], the oscillation circuit activating an initial oscillation operation [oscillation signal build-up] according to an enable signal [signal output of D-Q flip-flop 7, as applied to AND gate 14], and operating according to a high working voltage [Vcc] and a low working voltage [ground], comprising:

an enable circuit [AND gate 14 and D-Q flip-flop 14], outputting an initial oscillation signal [f1, further creating partial signals at the sources of transistors Q6 and Q7] after the initial oscillation operation according a feedback control signal [output of inverter 13 applied to AND gate 14];

an oscillator delay circuit [series of inverters comprising ring oscillator 12], coupled to the enable circuit, receiving the initial oscillation signal from the enable circuit (signal f1

feeding back to the gates of Q6 and Q7) and alternately generating a high level oscillation signal [located at the source of transistor Q6 of right-most inverter 13] oscillating in a high voltage area and a low level oscillation signal [located at the source of transistor Q7 of right-most inverter 13] oscillating in a low voltage area according the initial oscillation signal (as signal f1 drives ring 12 and inverter 13), wherein the high voltage area is between the high working voltage and a low-limit voltage [bias voltage at the gate of transistor Q6] higher than the low working voltage, and the low voltage area is between the low working voltage and an upper-limit voltage [bias voltage at the gate of transistor Q7] lower than the high working voltage; and

a feedback control network [right-most inverter 13], coupled to the oscillator delay circuit, integrating the high level oscillation signal and the low level oscillation signal as the feedback control signal [output of inverter 13, as applied to input of AND gate 14] and outputting the feedback control signal to the enable circuit.

Regarding **claims 4, 6, 12, and 14**, Fig. 2 of Nakajima shows the low power consumption oscillation circuit of claims 2 and 1 respectively, wherein the oscillator delay circuit comprises a plurality of delay circuits [each inverter identical to inverter 13 in series in ring 12].

Regarding **claim 7 and 15**, Fig. 2 of Nakajima shows the low power oscillation circuits of claims 6 and 14 respectively, wherein the delay circuits comprise:

a first delay circuit [inverter 13], coupled to the enable circuit; and

a plurality of backend delay circuits [series inverters in ring 12, driving inverter 13], the backend delay circuits comprising delay circuits connected in series, wherein a second delay circuit [inverter directly to left of inverter 13] is coupled to the first delay circuit, and an output delay circuit [inverter directly to left of inverter 13] is coupled to the feedback control network.

Regarding **claims 5, 8-9, 13 and 16-17**, Fig. 2 of Nakajima shows the low power oscillation circuits of claims 4, 12 and 15 respectively, wherein the delay circuits comprise:

a pull-up device [Pmos transistor Q5], coupled to the high working voltage, receiving the high level oscillation signal outputted from the enable circuit;

a pull-down device [Nmos transistor Q8], coupled to the low working voltage, receiving the low level oscillation signal outputted from the enable circuit;

a loading device [inverter formed by transistors Q6 and Q7], coupled to the pull-up and pull-down devices and disposed between the pull-up and pull-down devices;

a first output terminal [source of transistor Q6], coupled to the pull-up device and the loading device and disposed between the pull-up device and the loading device, outputting the high level oscillation signal to the feedback control network; and

a second output terminal [source of transistor Q7], coupled to the pull-down device and the loading device and disposed between the pull-down device and the loading device, outputting the low level oscillation signal to the feedback control network.

Regarding **claims 10-11 and 18-19**, Fig. 2 of Nakajima shows the low power consumption oscillation circuit of claims 6 and 14 respectively, wherein the feedback control network comprises a plurality of inverters [tri-state inverter 8 and inverter 13], the inverters comprising:

a plurality of inverters, each of the inverters comprising a P-type semiconductor device [Pmos transistor of inverter 8 and Pmos transistor Q6 of inverter 13] and an N-type semiconductor device [Nmos transistor of inverter 8 and Nmos transistor Q7 of inverter 13]; and

a plurality of external control inverters [tri-state inverter 8 and inverter 13], each of the external control inverters comprising a P-type semiconductor device, an N-type semiconductor device, an external P-type semiconductor device and an external N-type semiconductor device, wherein each of the inverters and each of the external control inverters are alternately coupled to each other in series.

Regarding **claim 21**, Fig. 2 of Nakajima shows the delay circuit of a low power oscillation circuit of claim 20, wherein the first signal [SG1] is the same as the second signal [SG2].

Regarding **claim 22**, Fig. 2 of Nakajima shows the delay circuit of a low power oscillation circuit of claim 20, wherein the pull-up device [Q5] comprises a Pmos transistor.

Regarding **claim 23**, Fig. 2 of Nakajima shows the delay circuit of a low power oscillation circuit of claim 20, wherein the pull-down device [Q8] comprises an Nmos transistor.

Regarding **claim 24**, Fig. 2 of Nakajima shows the delay circuit of a low power oscillation circuit of claim 20, wherein the loading device [inverter comprising transistors Q6 and Q7] is an active device (as power is applied to an consumed by said inverter).

Regarding **claim 25**, Fig. 2 of Nakajima shows the delay circuit of a low power oscillation circuit of claim 1, wherein the feedback control network comprises an inverter [13].

Regarding **claim 26**, Fig. 2 of Nakajima shows the delay circuit of a low power oscillation circuit of claim 25, wherein the inverter comprises a Pmos transistor [Q6] and an Nmos [Q7] transistor, which are coupled in series.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Porter et al. ***(US 6,724,218)***.

Regarding **claim 3**, Fig. 2 of Nakajima shows the low power consumption oscillation circuit of claim 2, except. "wherein the enable circuit comprises: a P-type semiconductor device combination, coupled to the high working voltage, outputting the high level oscillation signal according to the feedback control signal; an N-type semiconductor device combination, coupled to the low working voltage, outputting the high level oscillation signal according to the feedback control signal; and a loading device, coupled to the P-type semiconductor device combination and N-type semiconductor device combination and disposed between the P-type semiconductor device combination and N-type semiconductor device combination."

However, Fig. 18 and the abstract of Porter shows in more detail a NAND gate, which could be implemented in series with a 2nd NAND gate to achieve the AND gate [14] shown in Nakajima. This enable circuit comprises: a P-type semiconductor device combination [1808], coupled to the high working voltage, outputting the high level oscillation signal according to the feedback control signal; an N-type semiconductor device combination [nmos transistor inherent in an inverter, such as inverter 1610], coupled to the low working voltage, outputting the high level oscillation signal according to the feedback control signal; and a loading device, coupled to the P-type semiconductor device combination and N-type semiconductor device combination and disposed between the P-type semiconductor device combination and N-type semiconductor device combination.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Nakajima by including the particular AND

gate configuration of Porter for the purpose of obtaining desired trip characteristics of the AND gate for only enabling feedback when those trip characteristics are met.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James E. Goodley whose telephone number is 571-272-8598. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JG

Zandra V. Smith
Primary Examiner